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(81) Designated States: DE, GB, JP, US, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

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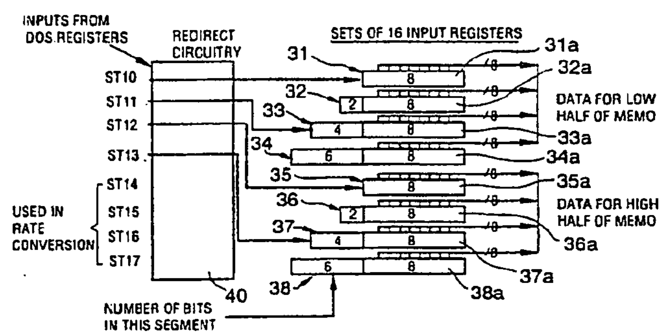
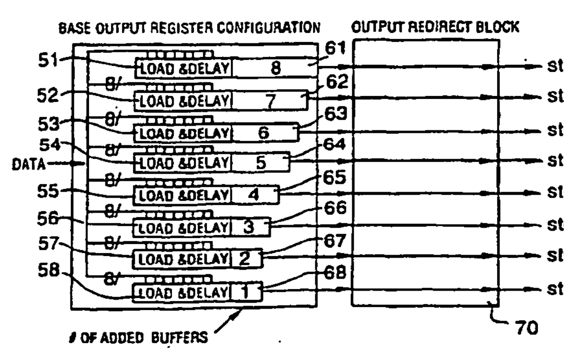
(54) Title: SERIAL BIT RATE CONVERTER FOR A TDM SWITCHING MATRIX

(57) Abstract

A time division switching matrix capable of effecting rate conversion comprises a plurality of serial inputs for connection to respective serial input links, each capable of carrying time division multiplexed PCM channels, a plurality of serial outputs for connection to respective serial output links, each capable of carrying time division multiplexed PCM channels, and a serial-to-parallel converter associated with each input for converting a serial input stream to parallel format, each said serial-to-parallel converter being independently configurable to produce the same net parallel throughput regardless of the bit rate of the associated input link. The output side of the switching matrix can be similarly configured.





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SERIAL BIT RATE CONVERTER FOR A TDM SWITCHING MATRIX.

This invention relates to a time division switching matrix capable of effecting rate conversion.

Many digital telephone systems are based on the transport of time multiplexed, serialized PCM (pulse coded modulation) encoded voice bytes. PCM is an 8 bit encoding scheme for digitizing an analog voice signal, sampled at 8 khz. Different telephone networks employ different degrees of multiplexing between the bytes flowing serially at a rate of 8 bits per 125 microseconds (the period of 8 khz.). Popular schemes include time division multiplexing of 32 voice channels (for a net data rate of 2.048 megabits per second), 64 voice channels (for 4.096 megabits per second) or 128 voice channels (for 8.192 megabits per second) onto single PCM highways.

Most if not all digital networks require switching between logical channels in the interconnected PCM highways. Hitherto this has been performed with rate conversion circuitry.

According to the present invention there is provided a time division switching matrix capable of effecting rate conversion comprising a plurality of serial inputs for connection to respective serial input links, each capable of carrying time division multiplexed PCM channels, a plurality of serial outputs for connection to respective serial output links, each capable of carrying time division multiplexed PCM channels, and a serial-to-

parallel converter associated with each input for converting a serial input stream to parallel format, each said serial-to-parallel converter being independently configurable to produce the same net parallel throughput regardless of the bit rate of the associated input link.

The invention allows for rate conversion in the switching matrix, for example, between PCM highways of 2.048 megabits per second, and 4.096 megabits per second, or 2.048 megabits per second and 8.192 megabits per second. It also allows for conversion from 8.192 megabits per second to 2.048 megabits per second, or 4.096 megabits per second and 2.048 megabits per second. With rate conversion, networks with differing serial backplanes can be interconnected.

In the preferred embodiment, the switching core of the device consists of a ram based time switch that switches 256 x 256 channel locations. During each 125 microsecond frame 256 bytes of incoming PCM data are written in sequence into a data ram. During the frame, 256 reads of the same memory fetch PCM data bytes, which are shifted out onto serial output links. The time at which the fetch occurs determines the output link and channel number that the PCM data is to be routed to.

The invention will now be described in more detail, by way of example only, with reference to the accompanying drawings, in which:

Figure 1 is a diagram showing the memory address timing for a switching matrix in accordance with the invention;

Figure 2 is a diagram showing the inputs shift registers for the 2Mb/s mode;

Figure 3 shows the input data stream redirects for the 4Mb/s mode;

Figure 4 shows the input data stream redirects for 8Mb/s mode;

Figure 5 shows the 2Mb/s configuration;

Figure 6 shows the output data stream redirects for the 4Mb/s mode;

Figure 7 shows the 8Mb/s timing;

Figure 8 shows the output data stream redirects for the 8Mb/s mode; and

Figure 9 is a block diagram of a switching matrix in accordance with the invention.

The switching matrix shown in Figure 9 comprises input Mux 1, 2 each containing reconfigurable shift registers and producing 8 bit parallel output on input buses 3, 4, 5, 6 connected directly to memories 7, 8, 11, 12, and through Mux 16 to memories 9,10. The memories are in turn are connected to parallel output buses 13. Output buses 13 are connected through data select switch 14 to

output Mux 15, which is connected to eight serial output links.

The switch also includes a counter 17, a frame counter 18, an address control unit 19, and low and high memories 20, 21.

At 2.048 megabits per second input and output, the switching matrix can switch between 8 physical input links with 32 time multiplexed PCM channels and 8 output links with 32 channels. As the speed of the input (output) data rate is increased, the number of input (output) is reduced by half, and the number of channels in the active links double. The switching memory always operates with a nominal 244 nanosecond cycle time.

The multiplexing of the data memory accesses is depicted in Figure 1, in which Foi is an 8khz framing pulse and C4i is a 4.096 Mhz clock that clocks the operation of the memories

Data memory writes are doubled up, i.e. 2 PCM bytes from the serial input are written in parallel to free up clock cycles for time multiplexed memory accesses.

Within this framework of accesses to the switching matrix core, incoming serial data is converted into a parallel format in sequence, to allow for 128 writes, of two bytes each, to be performed. This is accomplished by providing input shift registers that can be reconfigured to produce the same net parallel throughput independently of the serial bit rate of the input links. There are 8

serial input links available for input at 2.048 megabits per second operation. At 4.096 megabits per second only the first 4 are used, and at 8.192 megabits per second, only the first 2 are used. Blocking modes are also available that allow the use of more inputs.

The base input configuration, as used in the 2.048 megabit per second input data rate is shown in Figure 2, which shows serial inputs streams STI0 - STI7 input through redirect circuit 40 to a staggered length set of input shift registers 31 - 38. These are followed by a set of 8 tristateable latches with parallel data taps 31a - 38a. By staggering the length of the input shift registers, the time at which the input data is ready to be parallel loaded can bee effectively delayed, (i.e. when the output latches are enabled) in turn, from each latch set. The timing of this scheme is such that input stream 0&4 are written to data memory first, followed in sequence by 1 &5, 2&6 and 3&7, all in two 8 bit byte parallel format. This sequence is evident by the increasing length, and hence the time delay, associated with the ascending input stream pairs. The parallel data is written to the low (MSB=O) and high (MSB=I) halves of the data memory, allowing the use of only four write cycles in one internal channel cycle, based on the internal timing shown in Figure 1.

With input data at 4 megabits per second, the circuit operates without changing the base set of input registers seen in Figure 2, and within the constraints of the internal data memory write and read cycle timing as

shown in Figure 1. This is accomplished by redirecting the input streams to new sets of input latches, with the proper number of delay registers to align them with the internal enable / write timing pulses. This redirection for the 4 megabits per second mode is shown in Figure 3. The input sftm STIO continues into the first set of latches, while the input stream STI1 is redirected down one set, the input stream STI2 is redirected down two sets, and the input stream STI3 is redirected down three sets. This allows the data memory write cycles to remain in the same spot in the overall timing scheme, with only a minor modification to the coding of the input load pulses themselves. Instead of loading in an ascending pair sequence, the data is loaded from input latch sets 0&4, and then from 2&6 in a repeating sequence. Within a single internal 3.91 microsecond channel (32 of these in an internal 125 microsecond frame) there are 4 internal write cycles, but now the write data are loaded from latch sets 0&4 and 2&6 twice each, in the sequence 0&4,2&6,0&4,2&6. This necessitates a retiming of the output enable strobes of the input registers.

Referring now to Figure 4, for an 8 megabits per second input mode, only two input links are used, and these are redirected. The internal memory timing must be kept consistent, and the way the input data is latched and loaded adjusted to compensate for the change in serial input data rate. By redirecting the input stream to the latch set 4, load latch sets 0&4 can be parallel loaded repeatedly (4 times per internal channel) and

thereby the 8 megabits per second incoming data accommodated, with a consistent internal timing structure. The loading sequence is simply a repetition of 0&4,0&4,0&4,0&4 for one internal 3.91 microsecond channel. Of course, for all of these different modes, unique input shift register clocks must be generated to properly shift the input data at the desired data rate.

The output latch sets undergo a similar mapping strategy to accommodate the variable output rates in both standard and rate conversion modes. The output loads also base their timing on the internal data memory timing cycle seen in Figure 1, with 8 output register loads in one internal channel. These occur during the period labeled "data memory internal read accesses" in Figure 1. With 32 internal channels in one frame, and 8 output loads per channel, the desired 256 bytes of output data are achieved in one 125 microsecond frame. The base 2 megabit per second output configuration is seen in Figure 5. The output register sets consist of 8 bit loadable shift registers 51 - 58 followed by a variable length set of buffer registers. The variable length buffer registers play no part in the base 2 megabits per second mode. For this mode, the data is effectively loaded directly in to the "load & delay" section 51 - 58 and streams out with no additional delay. The staggered set of output registers are necessary to ensure that the data for each output stream aligns properly with the data stream channel boundary. The output of registers 61-68 passes to

output redirect circuit 70, where it emerges as 8 serial output streams STO0-STO-7.

It is evident from the decreasing number of register buffers added to the respective streams, which latch set is loaded first. The base loading sequence is 0,1,2,3,4,5,6,7, with the additional buffers delaying the channels that were loaded earlier, to force alignment with the output channel boundary.

In 4 megabits per second output operation, shown in Figure 6, with external serial 8 bit channel times of 1.95 microseconds (8 x 244 nanoseconds), extra delay elements are introduced in the "load & delay" block. The buffer registers are necessary to align the output channel data with the external output channel boundaries, consistent with the internal data memory read timing. For 4 megabits per second mode, the output data streams are delayed by eight additional 4.096 Mhz output shift clock cycles, aligning the data with the external output channel timing. In addition, the data streams are redirected as necessary to align each loaded PCM byte to its respective link and channel boundary. The same internal load pulses are used, but the load enables are modified to load each latch set twice in one internal 3.91 microsecond channel. The load sequence is 0,2,4,6,0,2,4,6. This accommodates the 4 megabits per second output data rate while allowing the internal memory access and shift register load pulse timing to remain unchanged.

For an 8 megabits per second output mode (Figure 8), a similar reconfiguration occurs. In order to align the outgoing data streams with the internal cycle timing, delay the loaded output data must be delayed by twenty-four additional 8.192 Mhz output shift clocks by default, instead of the 8 output clock cycles for the 4 megabits per second mode. The reasons for this are apparent from an inspection of Figure 7. The output streams must be delayed by the appropriate number of additional cycles to align with the channel boundary. This is achieved by loading output latch sets 1 and 5, and redirecting the resulting data streams. The output load sequence in one internal channel is 1,5,1,5,1,5,1,5. This allows the 8 megabits per second data rate on the two output streams to be met within the constraints of the internal timing cycle.

As shown in Figure 7, STO0, channel 4N is loaded at point A, but it cannot come out until point B. This time is shown by the bracket C in the output shift vclock stream. Consequently, 7+24 = 31 buffer flip-flops must be added for alignment, which is why STI0 is redirected to latch set 1 instead of 0.

It is important to note that the architecture of the design allows for independence between the input and output modes. The input write addressing is based solely on the internal timing, with a variable addressing structure converting the connect memory contents to the appropriate address for output data reads. As well, the connect memory addressing is dependent only on the output

mode, and is automatically adjusted to compensate for the selected output mode. In this way, the input and output modes are essentially independent, and so are easily reconfigurable around the internal timing, to make backplane as well as rate conversion modes possible. The architecture is also easily extensible, with the simple addition of a new input and output mode decoding, and a slight modification to the load timing circuitry.

CLAIMS:-

1. A time division switching matrix capable of effecting rate conversion characterized in that it comprises a plurality of serial inputs for connection to respective serial input links, each capable of carrying time division multiplexed PCM channels, a plurality of serial outputs for connection to respective serial output links, each capable of carrying time division multiplexed PCM channels, and a serial-to-parallel converter associated with each input for converting a serial input stream to parallel format, each said serial-to-parallel converter being independently configurable to produce the same net parallel throughput regardless of the bit rate of the associated input link.

2. A time division switching matrix as claimed in claim 1, characterized in that said serial-to-parallel converters are shift registers.

3. A time division switching matrix as claimed in claim 2, characterized in that said shift registers are of staggered length so as to delay the time when input data is ready to be parallel loaded.

4. A time division switching matrix as claimed in claim 3, comprising means for redirecting the input serial data streams to different shift registers with the required number of delay registers so as to align the input streams with internal enable/write timing pulses.

5. A time division switching matrix as claimed in claim 1, characterized in that it further comprises a parallel-

to-serial converter associated with each output for converting a parallel input stream to serial format for application to the associated output link, each said parallel-to-serial converter being independently configurable to permit the same net parallel throughput regardless of the bit rate of the associated output link.

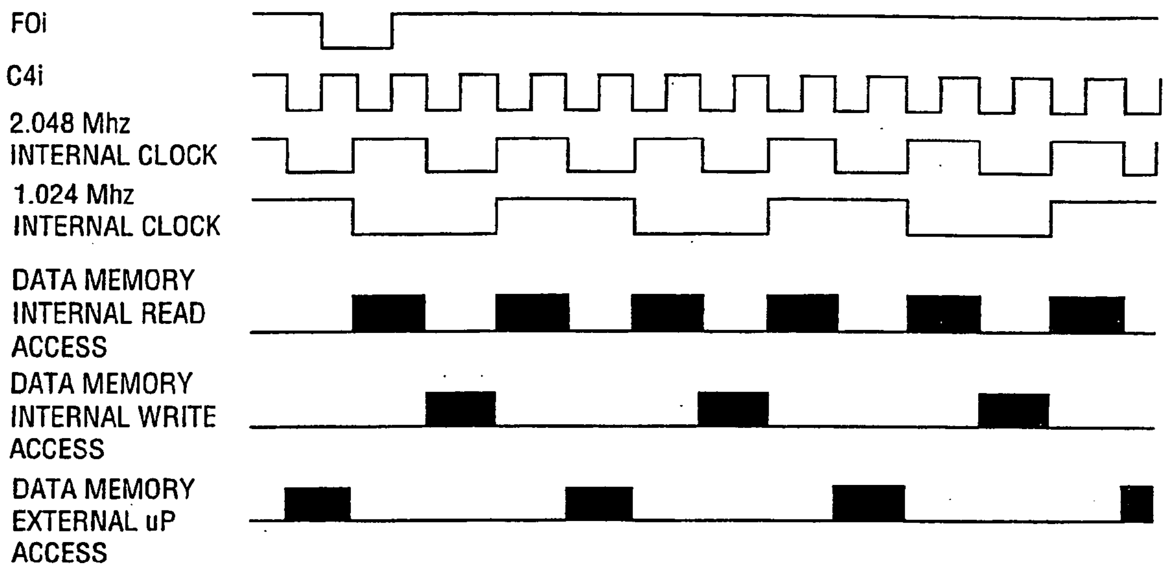
FOi
C4i
2.048 Mhz
INTERNAL CLOCK
1.024 Mhz
INTERNAL CLOCK
DATA MEMORY
INTERNAL READ
ACCESS
DATA MEMORY
INTERNAL WRITE
ACCESS
DATA MEMORY
EXTERNAL uP
ACCESS

FIG .1

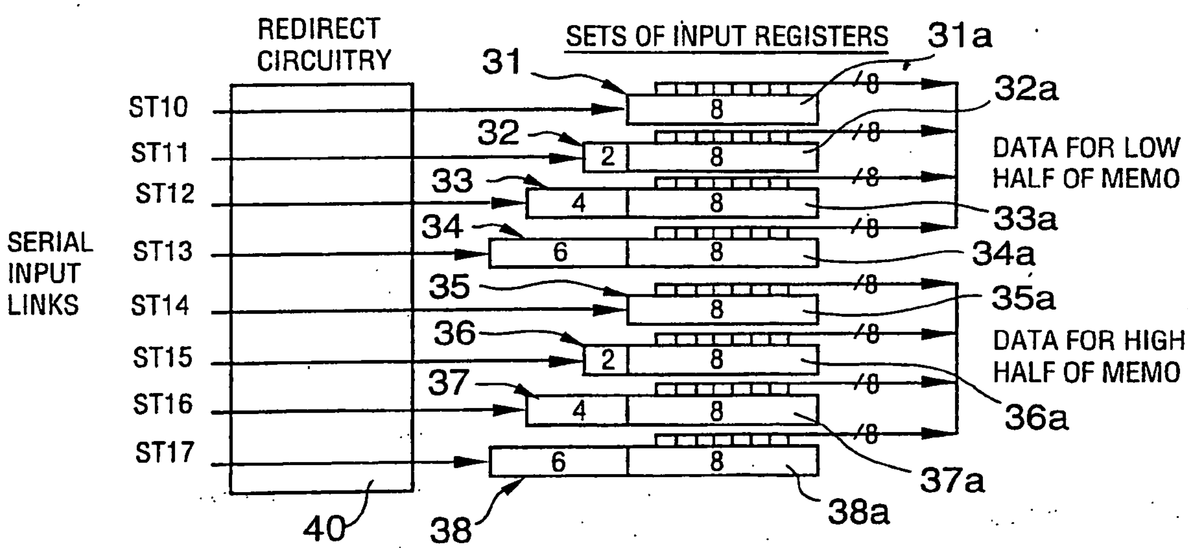
REDIRECT
CIRCUITRY
SETS OF INPUT REGISTERS
31
31a
32
32a
33
33a
34
34a
35
35a
36
36a
37
37a
38
38a
40
ST10
ST11
ST12
ST13
ST14
ST15
ST16
ST17
SERIAL
INPUT
LINKS
DATA FOR LOW
HALF OF MEMO
DATA FOR HIGH
HALF OF MEMO

FIG . 2

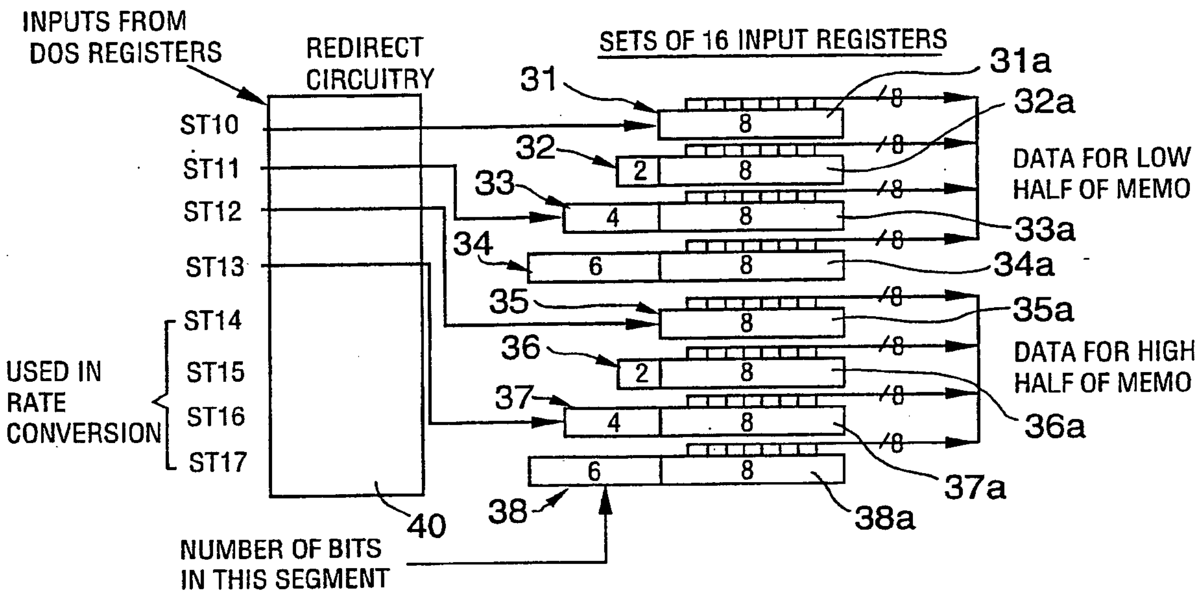
INPUTS FROM DOS REGISTERS
REDIRECT CIRCUITRY
SETS OF 16 INPUT REGISTERS
ST10
ST11
ST12
ST13
ST14
ST15
ST16
ST17
USED IN RATE CONVERSION
DATA FOR LOW HALF OF MEMO
DATA FOR HIGH HALF OF MEMO
NUMBER OF BITS IN THIS SEGMENT
31
31a
32
32a
33
33a
34
34a
35
35a
36
36a
37
37a
38
38a
40

FIG. 3

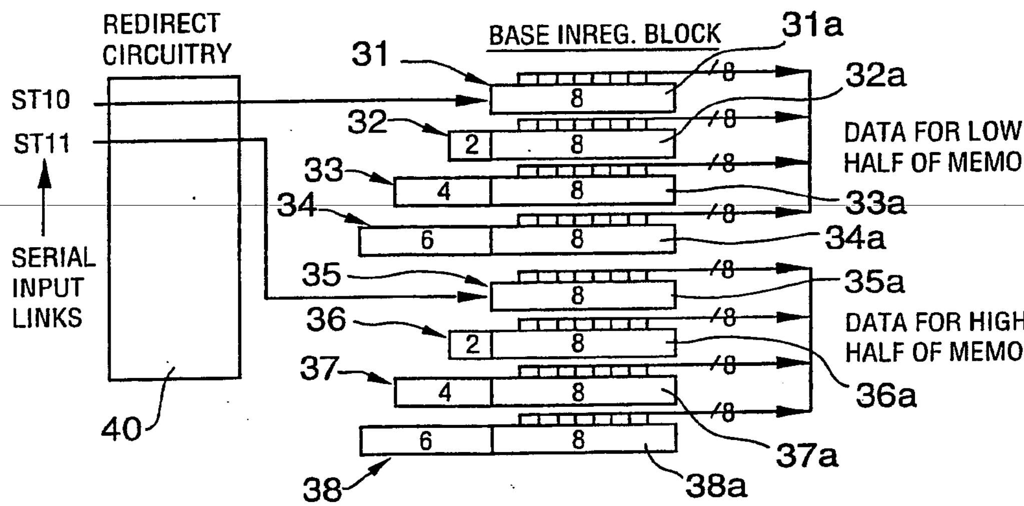
REDIRECT CIRCUITRY
BASE INREG. BLOCK
ST10
ST11
SERIAL INPUT LINKS
DATA FOR LOW HALF OF MEMO
DATA FOR HIGH HALF OF MEMO
31
31a
32
32a
33
33a
34
34a
35
35a
36
36a
37
37a
38
38a
40

FIG. 4

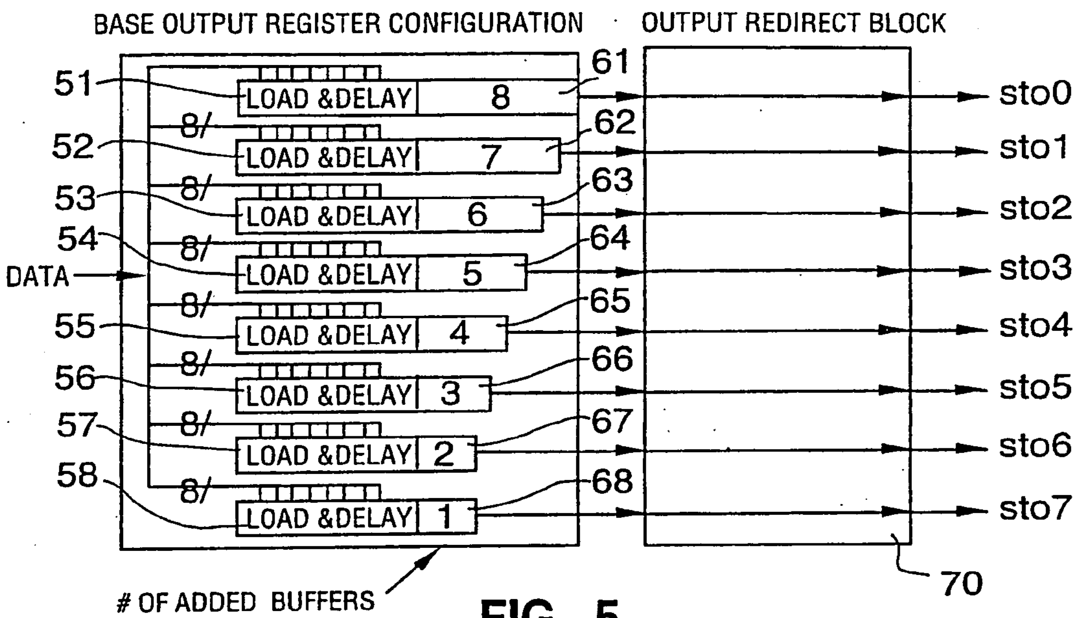
BASE OUTPUT REGISTER CONFIGURATION
OUTPUT REDIRECT BLOCK
51
52
53
54
55
56
57
58
DATA
8/
LOAD &DELAY
8
7
6
5
4
3
2
1
61
62
63
64
65
66
67
68
sto0
sto1
sto2
sto3
sto4
sto5
sto6
sto7
70
OF ADDED BUFFERS

FIG . 5

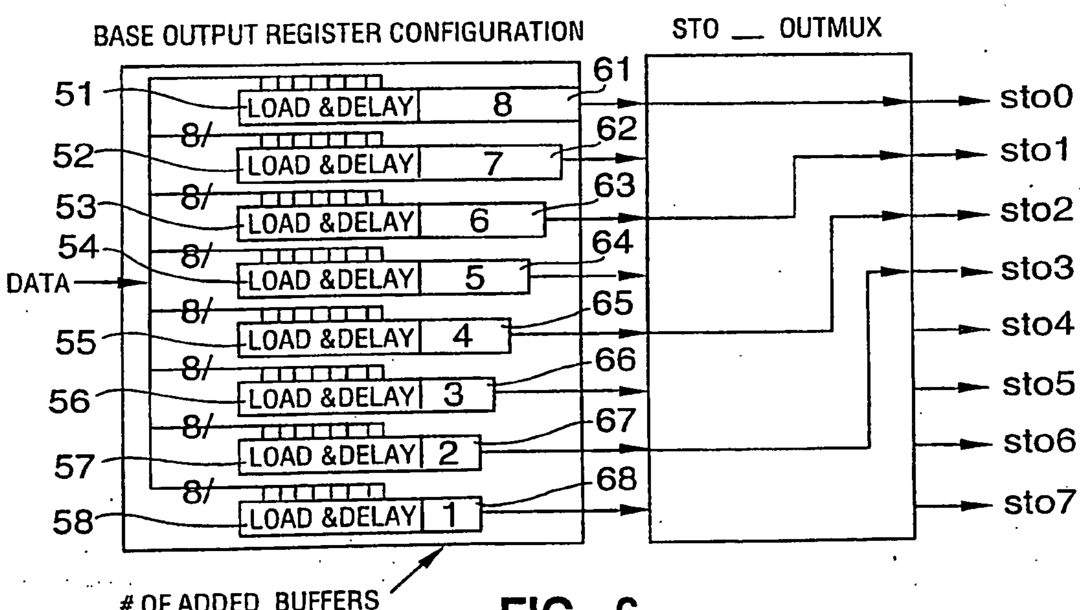
BASE OUTPUT REGISTER CONFIGURATION
STO _ OUTMUX
51
52
53
54
55
56
57
58
DATA
8/
LOAD &DELAY
8
7
6
5
4
3
2
1
61
62
63
64
65
66
67
68
sto0
sto1
sto2
sto3
sto4
sto5
sto6
sto7
OF ADDED BUFFERS

FIG . 6

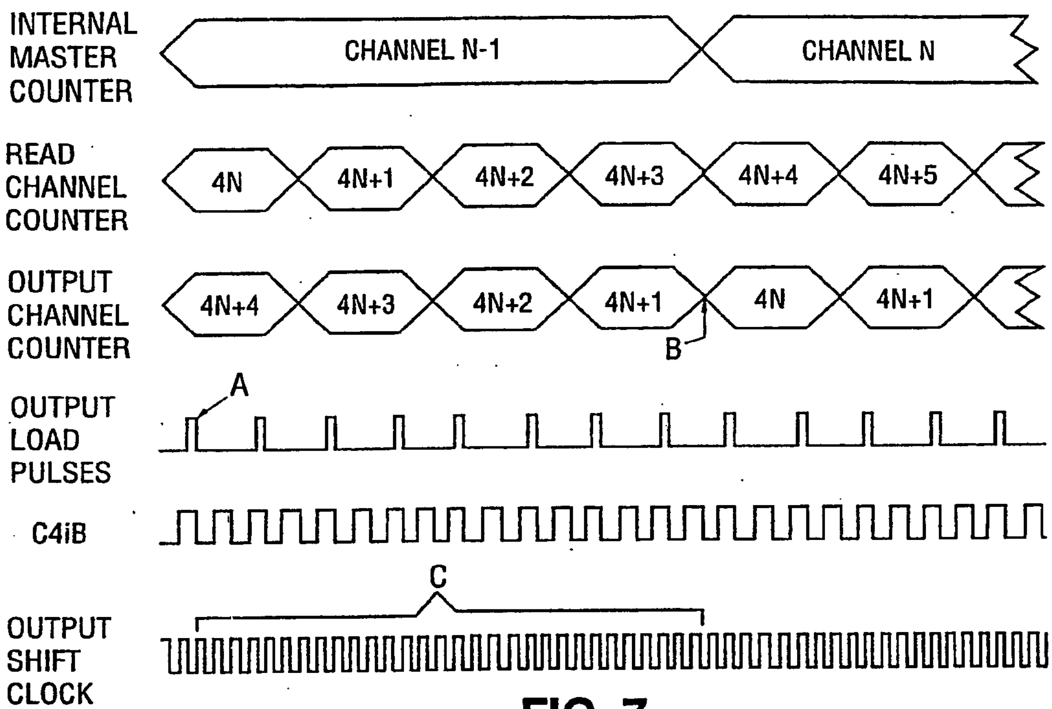
INTERNAL MASTER COUNTER
CHANNEL N-1
CHANNEL N
READ CHANNEL COUNTER
4N
4N+1
4N+2
4N+3
4N+4
4N+5
OUTPUT CHANNEL COUNTER
4N+4
4N+3
4N+2
4N+1
4N
4N+1
B
A
OUTPUT LOAD PULSES
C4iB
C
OUTPUT SHIFT CLOCK

FIG .7

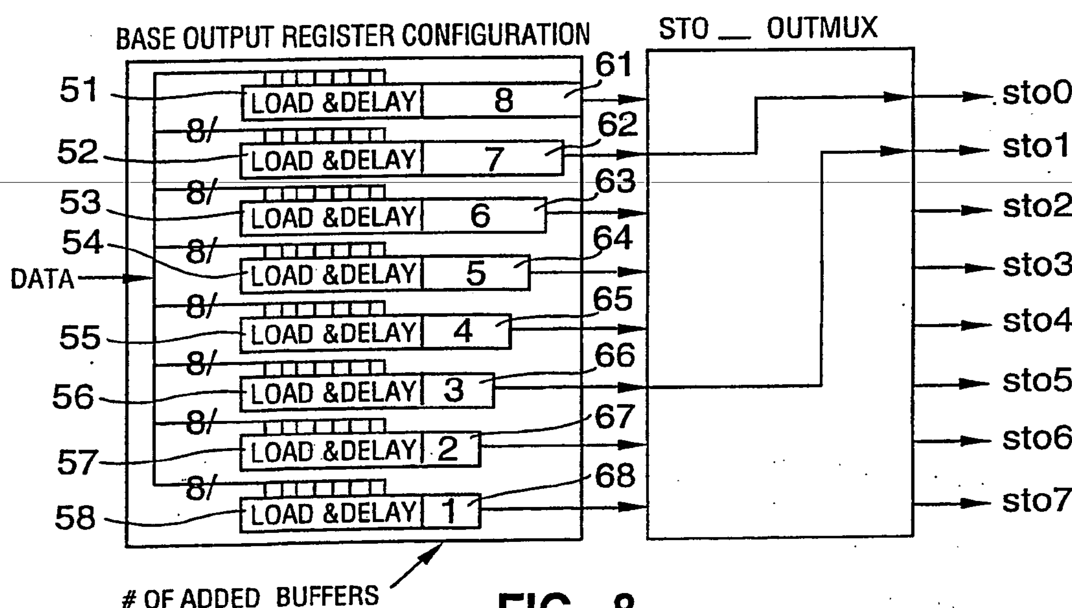
BASE OUTPUT REGISTER CONFIGURATION
STO __ OUTMUX
51
52
53
54
55
56
57
58
DATA
8/
LOAD &DELAY
8
7
6
5
4
3
2
1
61
62
63
64
65
66
67
68
sto0
sto1
sto2
sto3
sto4
sto5
sto6
sto7
OF ADDED BUFFERS

FIG . 8

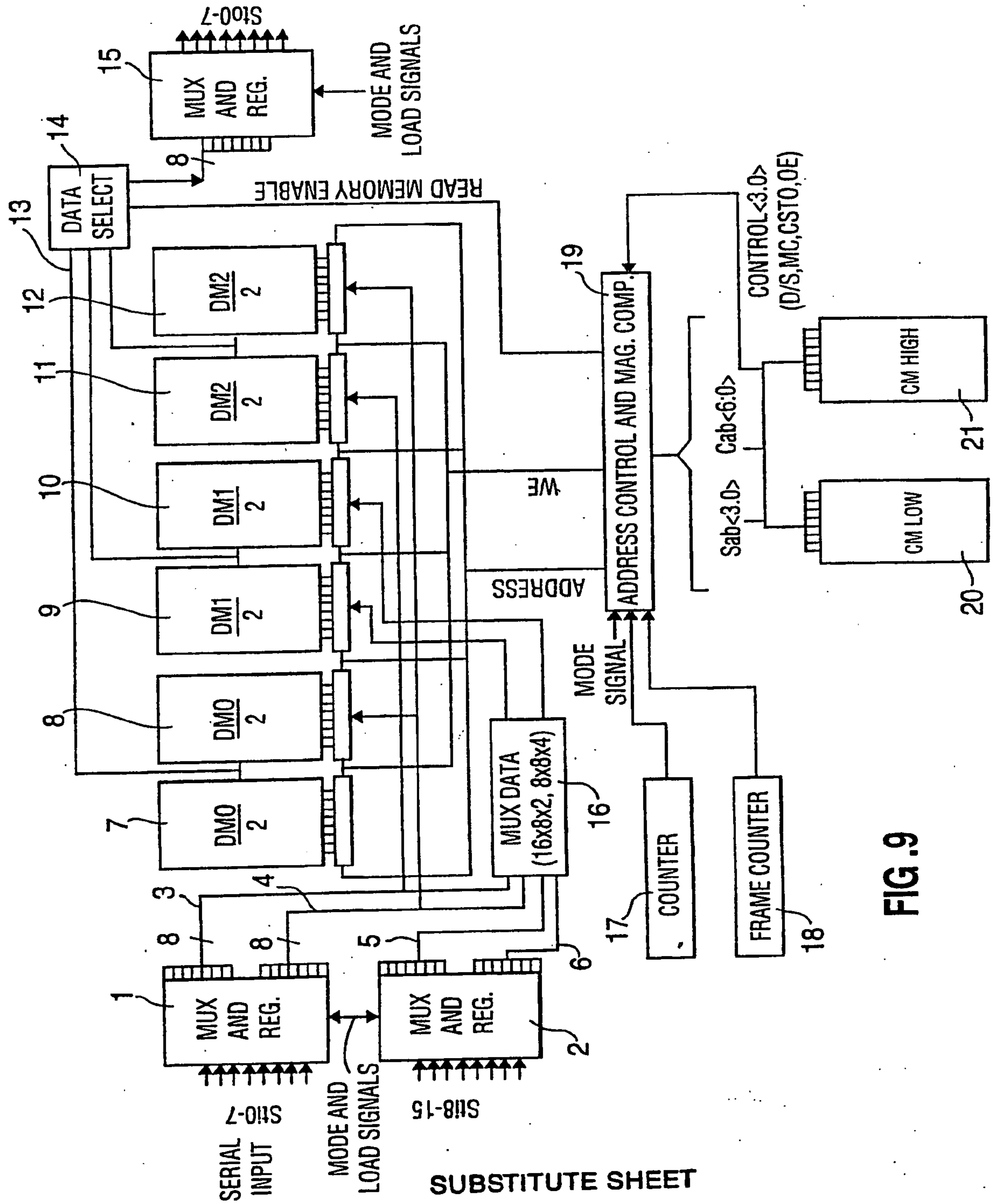
MUX AND REG.
MUX AND REG.
MUX AND REG.
SERIAL INPUT
SII0-7
SII8-15
MODE AND LOAD SIGNALS
MODE AND LOAD SIGNALS
DM0 2
DM0 2
DM1 2
DM1 2
DM2 2
DM2 2
DATA SELECT
READ MEMORY ENABLE
SIo0-7
MUX DATA (16x8x2, 8x8x4)
ADDRESS
WE
ADDRESS CONTROL AND MAG. COMP.
MODE SIGNAL
COUNTER
FRAME COUNTER
Sab<3.0>
Cab<6:0>
CONTROL<3.0> (D/S,MC,CSTO,OE)
CM LOW
CM HIGH
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21

FIG.9

INTERNATIONAL SEARCH REPORT

International Application No
PCT/CA 94/00377

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04Q11/08

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04Q

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	FR,A,2 376 572 (A. ROCHE) 28 July 1978 see the whole document ---	1-3,5
A	FR,A,2 265 240 (CGCT-LMT) 17 October 1975 see page 7, line 23 - page 11, line 16 ---	1-3,5
A	US,A,5 060 227 (FINLEY ET AL) 22 October 1991 see column 1, line 8 - line 13 see column 4, line 45 - column 5, line 4 see column 6, line 43 - line 45 see column 7, line 20 - line 41 see column 8, line 41 - line 59 --- -/--	1,5

[X] Further documents are listed in the continuation of box C.

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1

Date of the actual completion of the international search	Date of mailing of the international search report
28 October 1994	01. 11. 94
Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Authorized officer De Muyt, H

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	IEEE GLOBAL TELECOMMUNICATIONS CONFERENCE & EXHIBITION, vol.2, 28 November 1988, HOLLYWOOD (US) pages 1085 - 1089, XP112603 HAYASHI ET AL 'High-speed Program Controlled Multiplex circuit' see the whole document ---	1,5
A	PROCEEDINGS OF THE IEEE 1991 CUSTOM INTEGRATED CIRCUITS CONFERENCE - PAPER 3.4, 12 May 1991, SAN DIEGO (US) pages 1 - 4, XP295650 SHINAGAWA ET AL 'A Multi-speed Digital Cross-connect Switching VLSI using new circuit techniques in Dual Port RAMs' see the whole document ---	1,2,5
A	EP,A,0 453 129 (AT&T) 23 October 1991 see claims 1-19 ---	
A	EP,A,0 368 501 (STC PLC) 16 May 1990 see claims 1-10 -----	

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/CA 94/00377

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
FR-A-2376572	28-07-78	CA-A-	1136281	23-11-82
		DE-A,C	2758797	20-07-78
		GB-A-	1596178	19-08-81
		US-A-	4157458	05-06-79
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US-A-5060227	22-10-91	NONE		
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